FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))	ATTY. DOCKET NO. 200301779-2	SERIAL NO. Not Yet Assigned
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U. S. PATENT DOCUMENTS													
Examiner Initial		Patent Number							Issue Date	Patentee	Class	Sub-class	Filing Date (If Appropriate)
AH	AA	5	2	6	1	0	6	6	11/09/93	Jouppi et al.	395	425	03/27/90
AH	AB	5	3	1	7	7	1	8	05/31/94	Jouppi	395	425	01/25/93
AH	AC	5	7	5	8	1	8	3	05/26/98	Scales	395	825	07/17/96
AH	AD	5	7	6	1	7	2	9	06/02/98	Scales	711	148	07/17/96
AH	AE	5	7	8	7	4	8	0	07/28/98	Scales et al.	711	148	07/17/96
AH	AF	5	8	0	2	5	8	5	09/01/98	Scales et al.	711	154	07/17/96
AH	AG	5	8	0	9	4	5	0	09/15/98	Chrysos et al.	702	186	11/26/97
AH	AH	5	8	7	5	1	5	1	02/23/99	Mick	365	233	05/28/97
AH	AI	5	8	9	0	2	0	1	03/30/99	McLellan et al.	711	108	07/01/97
AH	AJ	5	8	9	3	9	3	1	04/13/99	Peng et al.	711	206	01/15/97
AH	AK	5	9	1	8	2	5	0	06/29/99	Hammond	711	205	05/05/95
AH	AL	5	9	1	8	2	5	1	06/29/99	Yamada et al.	711	207	12/23/96
AH	AM	5	9	2	3	8	7	2	07/13/99	Chrysos et al.	395	591	11/26/97
AH	AN	5	9	5	0	2	2	8	09/07/99	Scales et al.	711	148	02/03/97
AH	AO	5	9	6	4	8	6	7	10/12/99	Anderson et al.	712	219	11/26/97
AH	AP	5	9	8	3	3	2	5	11/09/99	Lewchuk	711	137	12/09/97
AH	AQ	6	0	0	0	0	4	4	12/07/99	Chrysos et al.	714	47	11/26/97
AH	AR	6	0	7	0	2	2	7	05/30/2000	Rokicki	711	117	10/31/97
AH	AS	6	0	8	5	3	0	0	07/04/2000	Sunaga et al.	711	168	09/19/97
AH	AT	5	9	5	3	5	3	8	09/14/1999	Duncan et al.	395	842	11/12/96
AH	AU	6	0	1	2	1	2	0	01/04/2000	Duncan et al.	710	129	03/18/99
AH	AV	6	3	3	8	1	2	3	01/2002	Joseph et al.	711	144	
AH	AW	5	7	7	8	4	3	7	07/1998	Baylor et al.	711	141	
AH	AX	6	0	2	6	4	6	1	02/2000	Baxter et al.	710	244	
AH	AY	5	9	5	3	5	1	2	09/1999	Cai et al.	712	205	

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OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)			
		AZ	*Alpha Architecture Reference Manual*, Third Edition, The Alpha Architecture Committee, 1998 Digital Equipment Corporation (21 p.), in particular pages 3-1 through 3-15
		BA	*A Logic Design Structure For LSI Testability*, E. B. Eichelberger et al., 1977 IEEE (Pages 462-468)
		BB	*Direct RDRAM™256/288-Mbit (512Kx16/18x32s)*, Preliminary Information Document DL0060 Version 1.01 (69 p.)
		BC	*Testability Features of AMD-K6™ Microprocessor*, R. S. Fetherston et al., Advanced Micro Devices (8 p.)
		BD	*Hardware Fault Containment in Scalable Shared-Memory Multiprocessors*, D. Teodosiu et al., Computer Systems Laboratory, Stanford University (12 p.), 1977
		BE	*Cellular Disco: resource management using virtual clusters on shared-memory multiprocessors*, K. Govil et al., 1999 ACM 1-58113-140-2/99/0012 (16 p.)
		BF	*Are Your PLDs Metastable?*, Cypress Semiconductor Corporation, March 6, 1997 (19 p.)
		BG	*Rambus® RIMM™ Module (with 128/144Mb RDRAMs)*, Preliminary Information, Document DL0084 Version 1.1 (12 p.)
		BH	*Direct Rambus™ RIMM™ Module Specification Version 1.0*, Rambus Inc., SL-0006-100 (32 p.), 2000
		BI	*End-To-End Fault Containment In Scalable Shared-Memory Multiprocessors*, D. Teodosiu, July 2000 (148 p.)
Examiner /Aurangzeb Hassan/ Date Considered 06/12/2006			
EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			